Bare Die fcPoP

Flip Chip Package-on-Package: fcVFBGA-PoPb, fcWFBGA-PoPb

Highlights

- Stacking fully tested memory and logic packages eliminates known good die (KGD) issues
- Package-on-package stacking provides flexibility in mixing and matching IC technologies
- Devices can be procured from multiple manufacturing sources
- Meets accepted package and board level reliability standards for chip scale packaging
- Flip chip enables higher performance, higher density, finer top PoP ball pitch and a smaller/thinner PoP solution

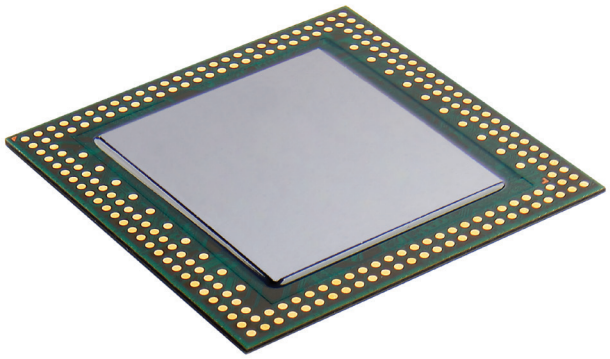
Features

- CuOSP or Ni/Au on bottom pads of bottom PoP (PoPb) with lead-free ball options
- Ni/Au on top memory interface pads of PoP
- Die thickness down to 60mm proven
- Supports 0.35mm minimum ball pitch on bottom/BGA pads and as low as 0.35mm pitch on top memory interface pads of PoPb
- Capable process with 40nm, 28m, 16nm and 10nm FAB technology in both lead-free and Cu pillar bumps
- Advanced CUF process maximizes allowable die size in package, with 30µm chip gap height
- Bottom PoP package thickness of 0.55mm max with 60mm thick flip chip die & 4 layer BU substrate or 2L/3L ETS
- Optimization of materials to meet warpage requirements during surface mount process
- Full in-house electrical, thermal and mechanical simulation and measurement capability
- Full in-house package and substrate design capability
- Turnkey solution including wafer bumping in both lead-free solder and Cu pillar bumps

Applications

We offer a complete PoP portfolio for a range of applications:

- PoPb: Application, baseband or multimedia processor for mobile handset and portable devices
- PoPt: Memory to support system and processor functions including DDR, Flash (NAND, NOR), SRAM and combinations thereof



Our Package-on-Package (PoP) family includes a stackable flip chip BGA as the bottom PoP package (PoPb). PoPb is typically an application processor or a baseband device with land pads placed on the top periphery of the package surface to enable the stacking of a second wire bond FBGA or PoP top (PoPt) above. PoPt, with memory devices stacked within, is assembled, tested and yielded independently. The two packages are combined by reflowing together (usually performed simultaneously) on the application board to form PoP (Z-interconnection with solder ball).

PoP has emerged as the preferred approach to integrate memory and logic in many advanced mobile and handheld applications. The bottom logic package and top memory package can be assembled, tested and yielded independently. This business model is preferred by end users as they can leverage their usual suppliers for these device types independently and have the flexibility to match logic processor and memory to support different applications.

We have always been at the forefront of 3D packaging and stacked die packaging. The wirebonded bottom PoP package was developed and introduced into production more than a decade ago. The bottom fcPoP provides the advantage of denser design with larger die size and higher number of IOs within the same PoP package body size / form factor as compared to the wirebonded PoP version. In addition, the use of fcPoP allows for potentially lower PoPb package height, thus reducing the total package stacked height post-SMT process. Improved device electrical performance can also be expected with the fcPoP package as with all other Flip Chip packages in comparison to wirebonded designs. Bare die fcPoP package offers the lowest cost PoP package type and can use down to 0.35mm memory interface (MI) pitch.

Specifications (fcPoP)

Die Thickness	Minimum 60mm
FC Bump Pitch	Minimum 140mm (Pb-free) Minimum 80mm/40mm (Cu/SnAg)
FC Bumps*	Pb-free, Cu pillar
Solder Balls	Sn/Ag/Cu (Pb-free ball)
Marking	Laser
Packing Options	JEDEC tray or tape & reel

*Refer to fcCuBE datasheet for PoP package details using Cu pillar interconnect.

Reliability

Moisture Sensitivity Level	JEDEC Level 2A, (60% RH/60°C), 120 hrs
Temperature Cycling	Condition B (-55°C/+125°C, 1000 cycles)
Temp/Humidity Cycling	85°C/85% RH, 1000 hrs
Highly Accelerated Stress Test	135°C/85% RH, 96 hrs
High Temperature Storage	150°C, 1000 hrs

Thermal Performance

Thermal behavior is determined by the exact configuration of the overall structure and the distribution of power dissipation among all of the die. During the package design process, we provide quick-turn thermal feasibility analysis and data as needed to help ensure proper thermal operation.

Package	Leads	Die Size (mm)	Power (W)	T_A (°C)	Airflow (m/s)	T_J (°C)	θja (°C/W)
12 x 12mm fcPoP	753	7 x 7 x 0.1	2	25.0	NC**	71.9	23.4
14 x 14mm fcPoP	641	8 x 8 x 0.1	2	25.0	NC**	70.0	22.5
15 x 15mm fcPoP	992	8.6 x 10.9 x 0.1					

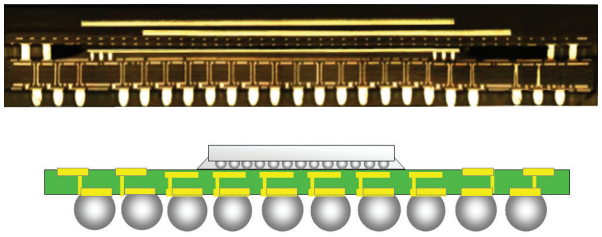
Notes: *Typical bottom fcPoP thermal performance. Data for bottom PoP only without the effect of top PoP package. Substrate 4 layer laminate build-up (1/2/1). Simulation data for package mounted on 4 layer PCB per JEDEC JES51-9 under natural convection. **NC=Natural Convection

Electrical Performance

The electrical behavior is highly dependent on the package layout and the substrate structures. 3D electrical simulation is used to predict the actual electrical behavior once designs are partially or fully completed. As expected, the electrical performance advantage of using flip chip over wire bond is seen in these packages.

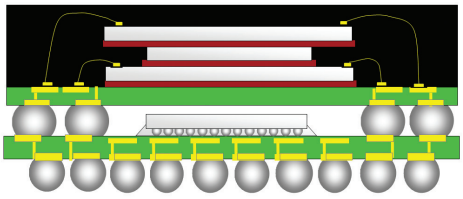
Cross Sections

Bottom fcPoP (PoPb)



fcVFBGA-PoPb

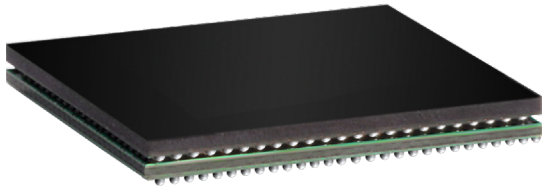
Pre-Stacked fcPoP (PoPb + PoPt)



TFBGA-PoPt-SD3 + fcVFBGA-PoPb

Package Configurations

Package	Wire Bond	Flip Chip Interconnect	Body Size (mm)	BGA Pitch (mm)	Top Pitch (mm)
Bare Die PoP	No	Pb-free	10x10 ~ 15x15	min 0.4	0.5
		Cu/Sn/Ag			0.4



Pre-Stacked fcPoP: Bare Die PoPb + Memory PoPt

Test Services

- Product Engineering support
- Probe capability
- Program generation / conversion
- Drop shipment available

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